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TOWNSEND AND TOWNSEND AND CREW LLP/ 015114
TWO EMBARCADERO CENTER
8TH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER	
CHEN, TSE W	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 04/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/880,734	CROSLAND ET AL.	
	Examiner	Art Unit	
	Tse Chen	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15,44 and 46-54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15,44 and 46-54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment dated March 3, 2005.

2. Claims 1-15, 44, and 46-54 are presented for examination. Applicant has canceled claims 16-43, and 45.

Claim Objections

3. Claims 44 and 48 are objected to because of the following informalities:

- As per claim 44, "the integrated circuit" in the last limitation should be "the programmable logic integrated circuit".
- As per claim 48, "the watchdog timer" should be "the watchdog timer circuit".

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Re Claims 1-2, 4-5, and 7-14

5. Claims 1-2, 4-5, and 7-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van de Steeg et al., US Patent 5479618, hereinafter Steeg, in view of Yokouchi et al., US Patent 4796211, hereinafter Yokouchi.

6. In re claim 1, Steeg discloses a method of operating a programmable logic integrated circuit [plc 29, 37] comprising:

- Loading an initial value [data] in a count register of a watchdog timer circuit [60] of the programmable logic integrated circuit [col.6, ll.17-27, ll.47-67; col.8, ll.49-59].
- Upon receiving a triggered signal [reset/clear] output in a reset logic block [fault logic circuit] of the programmable logic integrated circuit, causing reloading of configuration data from an external source [prom 25] into the programmable logic integrated circuit [col.3, ll.28-53; col.8, ll.49-59; col.9, ll.54].

7. Steeg did not discuss the details of the watchdog timer.

8. Yokouchi discloses a method of operating a programmable logic integrated circuit [cpu] comprising [col.1, ll.21-35]:

- Clocking a count register to advance the count register to a next value with each clock [counter advances in sync with the clocking that drives cpu execution].
- Periodically reloading the count register with an initial value [preset].
- When the stored count value held in the count register of the watchdog timer circuit reaches a final value [expiration], asserting a triggered signal output [interrupt].

9. It would have been obvious to one of ordinary skill in the art, having the teachings of Steeg and Yokouchi before him at the time the invention was made, to use the watch dog timer taught by Yokouchi for the programmable logic integrated circuit disclosed by Steeg as the watchdog timer taught by Yokouchi is a well known device suitable for use as the watchdog timer of Steeg. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to counter against problems associated with external noise, aging, etc. [Yokouchi: col.1, ll.6-13].

10. As to claim 2, Steeg discloses the method wherein the external source is a nonvolatile memory [prom 25].

11. As to claim 4, Yokouchi discloses the method wherein the final value causes an overflow condition for the count register of the watchdog timer circuit [col.1, ll.21-35; no preset causes overflow of a final value].

12. As to claim 5, Yokouchi discloses the method wherein the watchdog timer circuit increments the stored count values at each clock pulse [col.1, ll.36-47; start counting from 0].

13. As to claim 7, Yokouchi discloses the method wherein periodically reloading the count register comprises:

- Writing a magic value [data e1H] into a reload register of the watchdog timer circuit.
- When the magic value is received in the reload register, resetting the count register of the watchdog timer circuit to the initial value [col.1, ll.36-47].

14. As to claim 8, Yokouchi discloses the method wherein periodically reloading the count register comprises:

- Writing a first magic value [1eH] into a reload register of the watchdog timer circuit.
- When the first magic value is received in the reload register, reloading the count register of the watchdog timer circuit to the initial value [col.1, ll.36-47].
- After the first magic value is received in the reload register, permitting a subsequent reload [reset] of the count register when a second magic value [e1H] is written into reload register [col.1, ll.36-47].

15. As to claim 9, Yokouchi discloses the method comprising continually reloading the count register to the initial value by writing the first and second magic values to the reload register in sequence, alternately [col.1, ll.36-47].

16. As to claim 10, Steeg discloses the method comprising using the configuration data to configure an embedded processor portion [plc 29] and a programmable logic portion [plc 37] of the programmable logic integrated circuit [col.3, ll.28-53].

17. As to claim 11, Yokouchi discloses the method wherein to avoid asserting the triggered signal output, a periodic reload of the watchdog timer circuit should be performed during a timer period it takes the watchdog timer circuit to count from the initial value to the final value [col.1, ll.21-54].

18. As to claim 12, Yokouchi discloses the method wherein the period is less than about two minutes [e.g., 16 ms] [col.1, ll.36-47].

19. As to claim 13, Yokouchi discloses the method wherein the time period depends on clock frequency used to clock the watchdog timer circuit [col.1, ll.36-47; 16 ms at 12 Mhz].

20. As to claim 14, Yokouchi discloses the method wherein the initial value is 0 [col.1, ll.36-47]. The Examiner had taken Official Notice that it is well known in the art to have the final value that is a maximum count value permitted by the count register.

Re Claim 3

21. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Steeg and Yokouchi as applied to claim 1 above, and further in view of Harris et al., US Patent 6505341, hereinafter Harris.

22. In re claim 3, Steeg and Yokouchi disclose each and every limitation of the claim as discussed above in reference to claim 1. Steeg and Yokouchi did not disclose explicitly that the external source is a serial EPROM.

23. Harris discloses a method of operating a programmable logic integrated circuit [unit] [abstract] comprising an external source that is a serial EPROM [108] [fig.2; col.9, ll.57-65].

24. It would have been obvious to one of ordinary skill in the art, having the teachings of Harris, Steeg and Yokouchi before him at the time the invention was made, to use the serial EPROM taught by Harris for the external source disclosed by Steeg and Yokouchi as the serial EPROM taught by Harris is a well known device suitable for use as the external source of Steeg and Yokouchi. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to store configuration information [Harris: col.9, ll.57-65].

Re Claims 6 and 15

25. Claims 6 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Steeg and Yokouchi as applied to claim 1 above, and further in view of Frisch, US Patent 5721828.

26. Steeg and Yokouchi disclose each and every limitation of the claim as discussed above in reference to claim 1. Steeg and Yokouchi did not disclose decrementing the stored count or that the count register comprises 32 bits.

27. In re claim 6, Frisch discloses a method comprising a timer circuit [timer] that decrements the stored count value [col.28, ll.19-31].

28. It would have been obvious to one of ordinary skill in the art, having the teachings of Frisch, Steeg and Yokouchi before him at the time the invention was made, to use the timer circuit that decrements the stored count value taught by Frisch for the timer circuit disclosed by

Steeg and Yokouchi as the timer circuit taught by Frisch is a well known timer suitable for use as the timer circuit of Steeg and Yokouchi. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to time an event [e.g., interrupt] [Frisch: col.28, ll.15-22].

29. In re claim 15, Frisch discloses a method comprising a count register [counter register] that comprises 32 bits [col.27, ll.60-63; col.28, ll.28-31].

30. It would have been obvious to one of ordinary skill in the art, having the teachings of Frisch, Steeg and Yokouchi before him at the time the invention was made, to use the count register that comprises 32 bits taught by Frisch with the programmable logic circuit disclosed by Steeg and Yokouchi as the count register taught by Frisch is a well known count register suitable for use with the programmable logic circuit of Steeg and Yokouchi. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to hold the count value [Frisch: col.27, l. 60 – col.28, l.8].

Re Claims 44, 46–51, and 53

31. Claims 44, 46-51, and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yokouchi, in view of Van de Steeg.

32. In re claim 44, Yokouchi discloses a method of operating a programmable logic integrated circuit [cpu] comprising [fig.2; col.1, ll.36-54]:

- Clocking a watchdog timer circuit of the programmable logic integrated circuit [col.2, ll.45-54] to advance a count register of the watchdog timer circuit [enable the counter for free-running counting].

- Loading a first magic value [data 1eH] into a reload register [inherently, some kind of reload register in the broadest interpretation is needed to secure the value] of the watchdog timer circuit, which resets [initializes] the count register to an initial value.
- After loading the first magic value, loading a second magic value [data e1H] into the reload register, which causes the count register to reset the initial value [col.1, ll.36-47].
- After loading the first magic value into the reload register, loading a value other than the second magic value into the reload register, which causes the watchdog timer circuit to generate a triggered signal [carry signal] [col.1, ll.48-54; incorrect combination written will cause reset].
- Receiving the triggered signal in a reset logic block [reset receiving circuit 5] of the programmable logic integrated circuit, which causes a reloading of configuration data [from address 0] into the programmable logic integrated circuit [col.1, ll.36-54].

33. Yokouchi did not discuss the details of loading configuration data.

34. Steeg discloses a method of operating a programmable logic integrated circuit [plc 29, 37] comprising:

- Receiving a triggered signal [reset/clear] in a reset logic block [fault logic circuit] of the programmable logic integrated circuit, which causes a reloading of configuration data from an external source [prom 25] into the programmable logic integrated circuit [col.3, ll.28-53; col.8, ll.49-59; col.9, ll.54].

35. It would have been obvious to one of ordinary skill in the art, having the teachings of Steeg and Yokouchi before him at the time the invention was made, to include the external source for configuration data taught by Steeg for the programmable logic integrated circuit

disclosed by Yokouchi as the external source for configuration data taught by Steeg is very well known for use with the programmable logic integrated circuit of Yokouchi. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to have a software re-configurable system that would be more flexible in adapting to changes in operations [Steeg: col.2, ll.2-29].

36. As to claim 46, Steeg discloses each and every limitation of the claim as discussed above in reference to claim 10.

37. As to claim 47, Steeg discloses the method wherein the watchdog timer circuit [60] is located in an embedded processor portion [plc 29] and the reset logic block [fault logic 78] is located in a programmable logic portion [plc 37] of the programmable logic integrated circuit [fig.2, 4-5].

38. As to claim 48, Yokouchi discloses the method comprising allowing the count register of the watchdog timer circuit to advance to a final value [fixed time; e.g., 16 ms] before the first or second magic values are loaded, which causes the watchdog timer circuit to generate the triggered signal [col.1, ll.36-54].

39. As to claim 49, Yokouchi discloses the method wherein the initial value is 0 [col.1, ll.36-47].

40. As to claim 50, the Examiner had taken Official Notice that it is well known in the art to have an initial value that is a value other than 0.

41. As to claim 51, Yokouchi discloses the method wherein the first magic value [1eH] is different from the second magic value [e1H] [col.1, ll.36-47].

42. As to claim 53, see discussion above in reference to claim 14.

Re Claim 52

43. Claim 52 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yokouchi and Steeg as applied to claims 48 above, and further in view of Muller, US Patent 6298360.

44. In re claim 52, Yokouchi and Steeg disclose each and every limitation of the claim as discussed above in reference to claim 48. Yokouchi and Steeg did not disclose explicitly that the final value is user-selectable.

45. Muller discloses a method comprising a value that is user-selectable [col.6, ll.30-46].

46. It would have been obvious to one of ordinary skill in the art, having the teachings of Muller, Yokouchi and Steeg before him at the time the invention was made, to modify the programmable logic integrated circuit taught by Yokouchi and Steeg to include the teachings of Muller, in order to obtain the final value that is user-selectable. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to initialize a timer [Muller: col.6, ll.30-46].

Re Claim 54

47. Claim 54 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yokouchi and Steeg as applied to claims 44 above, and further in view of Laiho et al., US Patent 6754830, hereinafter Laiho.

48. In re claim 54, Yokouchi and Steeg disclose each and every limitation of the claim as discussed above in reference to claim 44. Yokouchi and Steeg did not discuss the details of a debug mode.

49. Laiho discloses a method wherein in a debug mode, the count register [watchdog register] does not advance [col.4, ll.27-41].

50. It would have been obvious to one of ordinary skill in the art, having the teachings of Laiho, Yokouchi and Steeg before him at the time the invention was made, to modify the programmable logic integrated circuit taught by Yokouchi and Steeg to include the teachings of Laiho, in order to not advance the count register in debug mode. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to perform debugging [Laiho: col.4, ll.27-41].

Response to Arguments

51. All rejections of claim limitations as filed prior to Amendment dated March 3, 2005 not argued in entirety or substantively in response filed as said Amendment have been conceded by Applicant and the rejections are maintained from henceforth.

52. Applicant's arguments filed March 3, 2005 have been fully considered but they are not persuasive.

53. Regarding claim 1, Applicant alleges that the references "do not teach or suggest a programmable logic integrated circuit... in fact, Steeg teaches quite the opposite... Steeg describes a I/O module with integrated circuitry, which refers to an electronic circuit board with integrated circuits". Applicant essentially made general allegations without any related or clear and convincing support. Examiner invites Applicant to read/review 37 CFR 1.111 in order to comply with the expected constructs of an argument for a reply to an Office Action.

54. Firstly, Applicant proceeds to support the allegation by referencing column 3, line 54 of Steeg in asserting that the "two ***programmable logic circuits*** 29 and 37 may be integrated circuits such as provided in a ***Xilinx*** Inc. data book... there are two integrated circuits, not a programmable logic integrated circuit as in the claim". Examiner notes that Applicant

conveniently left out the rest of the paragraph from column 3, lines 54-67 in which the integrated circuit is described as a programmable logic circuit [logic blocks configured or programmed accordingly] in relation to Xilinx [known for making programmable logic circuits]. Applicant should know that this is not an acceptable way to form support for arguments.

55. Secondly, Applicant attempts to further support the allegation by referencing column 4, line 45 of Steeg that describes "the microelectronic processor as being the model 69 HC001 integrated circuit from Motorola Semiconductor". Applicant then halted completely in further explaining the significance of the cited support in relation to the allegation. Examiner is perplexed as to the point of this cited support as the rejection of the contending limitation was not based on the cited microelectronic processor, but on the programmable logic circuit [29, 37].

56. Thirdly, Applicant asserts that "nowhere does Yokouchi discuss a programmable logic integrated circuit" without even refuting Examiner's position that the CPU cited constitutes a programmable logic integrated circuit. Examiner invites Applicant to read either the previous or instant Office Action in reference to the rejection.

57. Regarding claim 1, Applicant alleges that the references do not teach or suggest "upon receiving the triggered signal output in a reset logic block of the programmable logic integrated circuit, causing reloading of configuration data from an external source into the programmable logic integrated circuit... the present invention is completely different from Steeg... the watchdog timer circuit and reset logic block reside on the programmable logic integrated circuit... the technique of the invention does not require two different programmable logic circuits".

58. Firstly, Examiner reminds Applicant that Examiner specifically cited the programmable logic circuit to constitute both 29 and 37 as it is well known in the art to combine multiple circuitries into one [hence, the term ***integrated*** circuit].

59. Secondly, Applicant's claim language did not require the watchdog timer circuit and reset logic block to reside on the programmable logic integrated circuit [until Applicant's limiting admission]. Examiner reminds Applicant that the claim reads "a reset logic block ***of*** the programmable logic integrated circuit". The key term "***of***" is a relative possessive term indicating some kind of relationship ***without*** a clear and distinct indication of boundary [e.g., the pencil ***of*** Mel does not absolutely mean the pencil is on or with Mel as the pencil could be with somebody else]. In this respect, the reset [fault] logic block can be ***of*** *programmable* logic circuit 37 [i.e., the programmable logic circuit without combined 29, 37] in that a contextual relationship can be established between the two entities.

60. As demonstrated, Applicant's arguments are not persuasive and the rejections are respectfully maintained.

61. Applicant's arguments with respect to claim 44 have been considered but are moot in view of the new ground(s) of rejection as necessitated by amendment.

Conclusion

62. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tse Chen
April 1, 2005

JOHN R. COTTINGHAM
PRIMARY EXAMINER